WHAT IS CLAIMED IS:

1. A method of forming a clamping plate for a multi-polar electrostatic chuck, comprising:

forming a first electrically conductive layer over a semiconductor platform and defining a plurality of portions of the first electrically conductive layer which are electrically isolated from one another;

forming a first electrically insulative layer over the first electrically conductive layer, the first electrically insulative layer comprising a top surface having a plurality of MEMS protrusions extending a first distance therefrom; and

forming a plurality of poles electrically connected to the respective plurality of portions of the first electrically conductive layer, wherein a voltage applied between the plurality of poles is operable to induce an electrostatic force in the clamping plate.

2. The method of claim 1, wherein forming the first electrically conductive layer comprises forming a polysilicon layer over the semiconductor platform.

3. The method of claim 2, wherein forming the first electrically conductive layer further comprises forming a metal layer over the polysilicon layer.

4. The method of claim 1, wherein the first electrically conductive layer is formed over a top surface of the semiconductor platform, the method further comprising forming a second electrically conductive layer over a bottom surface of the semiconductor platform, wherein a plurality of portions of second

electrically conductive layer are defined which are electrically insulated from one another.

5. The method of claim 4, wherein the first electrically conductive layer and the second electrically conductive layer are formed generally concurrently.

6. The method of claim 4, further comprising forming a plurality of vertical interconnects electrically connecting the plurality of portions of the first electrically conductive layer to the respective plurality of portions of the second electrically conductive layer.

7. The method of claim 6, wherein forming the plurality of vertical interconnects comprises forming a plurality of sidewall contacts over a sidewall of the semiconductor platform, wherein the plurality of sidewall contacts are electrically isolated from one another, and wherein the plurality of sidewall contacts electrically connect the respective plurality of portions of the first electrically conductive layer and the second electrically conductive layer.

8. The method of claim 7, wherein the forming the plurality of sidewall contacts comprises a deposition of an electrically conductive material over the sidewall of the semiconductor platform.

9. The method of claim 8, wherein the forming the plurality of sidewall contacts comprises depositing one or more of polysilicon, tungsten silicide, tungsten, or titanium.

10. The method of claim 6, wherein the formation of the first electrically conductive layer, the second electrically conductive layer, and the plurality of sidewall contacts are formed generally concurrently.

11. The method of claim 4, wherein forming the second electrically conductive layer comprises depositing one or more of tungsten silicide, tungsten, or titanium.

12. The method of claim 4, further comprising forming a base plate over the second electrically conductive layer, wherein the base plate is operable to transfer thermal energy from the substrate through the semiconductor platform to the base plate.

13. The method of claim 12, wherein the forming the base plate comprises forming a third electrically conductive layer having a plurality of portions electrically isolated from one another thereon, and electrically connecting the plurality of portions of the third electrically conductive layer to the respective plurality of portions of the third electrically conductive layer.

14. The method of claim 13, wherein forming the plurality of poles comprises bonding a plurality of electrodes to the respective plurality of portions of the third electrically conductive layer.

15. The method of claim 13, wherein the base plate comprises an amorphous silicon plate having an oxide layer formed thereover, wherein the third electrically conductive layer is formed over the oxide layer.

16. The method of claim 13, wherein forming the third electrically conductive layer comprises depositing one or more of tungsten silicide, tungsten, or titanium.

17. The method of claim 12, wherein forming the base plate comprises evaporating one or more metals onto the plurality of portions of the second electrically conductive layer.

18. The method of claim 12, wherein forming the base plate comprises vacuum brazing the base plate to the second electrically conductive layer.

19. The method of claim 12, wherein forming the base plate comprises applying an electrically conductive epoxy between the base plate and the second electrically conductive layer.

20. The method of claim 12, further comprising forming one or more fluid conduits through the base plate, wherein a cooling fluid is operable to flow therethrough.

21. The method of claim 12, further comprising forming a heat source within the base plate, wherein the heat source is operable to selectively heat the clamping plate.

22. The method of claim 1, wherein forming the first electrically conductive layer comprises depositing one or more of tungsten silicide, tungsten, or titanium.

23. The method of claim 1, wherein the semiconductor platform comprises a silicon substrate.

24. The method of claim 1, wherein the first electrically insulative layer is comprised of silicon dioxide.

25. The method of claim 1, further comprising forming one or more gas distribution grooves in the first electrically insulative layer, the first electrically conductive layer, and the semiconductor platform.

26. The method of claim 25, wherein forming the one or more gas distribution grooves comprises etching the first electrically insulative layer, the first electrically conductive layer, and the semiconductor platform.

27. The method of claim 25, further comprising forming one or more gas distribution holes through the semiconductor platform, the first electrically conductive layer, and the first electrically insulative layer, wherein at least one of the one or more gas distribution holes is formed through at least one of the one or more gas distribution grooves.

28. The method of claim 27, wherein forming the one or more gas distribution holes comprises a reactive ion etch of the first electrically insulative layer, the first electrically conductive layer, and the semiconductor platform.

29. The method of claim 1, wherein forming the plurality of MEMS protrusions further comprises:

forming a mask over the first electrically insulative layer, wherein the mask

generally defines a plurality of valleys over the top surface of the semiconductor substrate;

etching the first electrically insulative layer in the plurality of valleys; and

removing the mask, therein defining the plurality of MEMS protrusions between the plurality of valleys.

30. The method of claim 29, wherein etching the first electrically insulative layer uses the first electrically conductive layer as an etch stop.

31. The method of claim 29, further comprising forming a protective layer over the semiconductor platform after the first electrically insulative layer is formed thereover, and wherein etching the first electrically insulative layer uses the protective layer as an etch stop.

32. The method of claim 31, wherein forming the protective layer comprises depositing a nitride layer over the first electrically conductive layer and the semiconductor platform.

33. The method of claim 31, further comprising removing the protective layer on a bottom surface of the semiconductor platform.

34. The method of claim 1, wherein forming the first electrically conductive layer comprises forming a polysilicon layer over the semiconductor substrate.

35. The method of claim 1, wherein the plurality of MEMS protrusions are formed such that a substrate is operable to contact the plurality of MEMS

protrusions, therein defining a protrusion contact area, wherein a ratio of the protrusion contact area to a surface area of the substrate is between about 0.02 and 0.2.

36. The method of claim 35, wherein the ratio of the protrusion contact area to the surface area of the substrate is approximately 0.10.

37. The method of claim 1, wherein the first distance is approximately 1 micron.

38. The method of claim 1, further comprising forming a temperature sensor hole through the clamping plate, and inserting a temperature sensor into the temperature sensor hole.

39. The method of claim 1, wherein the semiconductor platform comprises a mosaic of a plurality of semiconductor segments.

40. The method of claim 39, wherein the mosaic of the plurality of semiconductor segments are comprised of doped silicon.

41. The method of claim 39, wherein forming the first electrically conductive layer over the semiconductor platform comprises forming the first electrically conductive layer over the plurality of semiconductor segments, wherein each of the plurality of portions of the first electrically conductive layer is formed over one or more of the plurality of semiconductor segments.

42. The method of claim 39, further comprising inserting an electrical insulator between each of the plurality of portions of the first electrically conductive layer formed over the plurality of semiconductor segments.

43. The method of claim 42, wherein the electrical insulator comprises a ceramic spacer.

44. The method of claim 1, further comprising forming a protective layer over the semiconductor platform after the first electrically insulative layer is formed thereover.

45. The method of claim 44, wherein forming the protective layer comprises depositing a nitride layer over the first electrically insulative layer and the semiconductor platform.

46. The method of claim 44, further comprising removing the protective layer on a bottom surface of the semiconductor platform.

47. The method of claim 1, wherein forming the first electrically conductive layer comprises a chemical vapor deposition of an electrically conductive material.

48. The method of claim 47, wherein forming the first electrically conductive layer comprises a chemical vapor deposition of tungsten silicide.

49. The method of claim 1, wherein the semiconductor platform comprises a silicon substrate having an oxide formed thereover.